Amendments to the Specification:

Please replace paragraph [0001] with the following amended paragraph:

[0001] ~~bk2E0012003032631.~~ 1. Field of the Invention ~~bk2E001200303263 The present invention relates to a bus, and more particularly, to a noise-proof bus circuit capable of diminishing noises in a clock signal transmitted over the bus.~~

Please add the following new paragraph after paragraph [0001]:

[0001.1] The present invention relates to a bus, and more particularly, to a noise-proof bus circuit capable of diminishing noises in a clock signal transmitted over the bus.

Please replace paragraph [0002] with the following amended paragraph:

[0002] ~~bk2E0012003032642.~~ 2. Description of the Prior Art ~~bk2E001200303264 In an electronic circuit, a signal transmitted over a conduction line is vulnerable to noises. In general, if the signal is a data signal transmitted over a data bus, noises interfering the data signal are negligible in determining the data signal. However, if the signal is a clock signal transmitted over a clock bus, any glitch in the clock signal may malfunction the electronic circuit.~~

Please add the following new paragraph after paragraph [0002]:

[0002.1] In an electronic circuit, a signal transmitted over a conduction line is vulnerable to noises. In general, if the signal is a data signal transmitted over a data bus, noises interfering the data signal are negligible in determining the data signal. However, if the signal is a clock signal transmitted over a clock bus, any glitch in the clock signal may malfunction the electronic circuit.

Please replace the Abstract with the following amended paragraph:

~~OLE_LINK1~~ A noise-free bus circuit for diminishing noises of an original clock signal over a bus. The noise-free bus circuit has a connection wire module and a voltage detection circuit. The connection wire module includes the bus and a conduction wire disposed along the bus. The bus has a first end connected to the original clock signal while the conduction wire has a first end connected to a reference voltage. The voltage detection circuit is electrically connected to second ends of the bus and the conduction wire for generating an amended clock signal by determining a voltage difference between voltages at the second ends of the bus and of the conduction wire, the amended clock signal being equivalently equal to the original clock signal without the noises.